UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,648	12/03/2001	Dale E. Gulick	2000.051600	8012

23720 7590 09/20/2006

WILLIAMS, MORGAN & AMERSON
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER
CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,648	GULICK, DALE E.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) *31-40,51-54,56-74 and 76-85* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30, 41-50, 55, and 75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the Applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the Applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3, 4, 5, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 30, 41, 42, 43, 44, 45, 46, 47, 48, 49, and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication Number 2002/0194415 to Lindsay et al. ("Lindsay").

3. In reference to Claim 1, Lindsay discloses a microcontroller (See Figure 8 Number 825) configurable as either an Alert Standard Format master or an Alert Standard Format slave (See Paragraphs 12-15 and 86), wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave (See Paragraph 90), wherein the microcontroller is further configured as an

Advanced Configuration and Power Interface controller (See Paragraphs 74, 75, 83, and 96).

4. In reference to Claim 2, Lindsay discloses the limitations as applied to Claim 1 above. Lindsay further discloses that the microcontroller is configured as the Alert Standard Format master (See Paragraph 90).

5. In reference to Claim 3, Lindsay discloses the limitations as applied to Claim 2 above. Lindsay further discloses that the microcontroller is coupled to an SMBus, and the microcontroller is further configured to receive Alert Standard Format status data from Alert Standard Format devices over the SMBus (See Paragraph 91).

6. In reference to Claim 4, Lindsay discloses the limitations as applied to Claim 1 above. Lindsay further discloses that the microcontroller is configured as the Alert Standard Format slave (See Paragraph 90).

7. In reference to Claim 5, Lindsay discloses the limitations as applied to Claim 4 above. Lindsay further discloses that the microcontroller is configured to receive status data from one or more Alert Standard Format devices, wherein the microcontroller is further configured to forward the status data from the one or more Alert Standard Format devices to the Alert Standard Format master (See Paragraph 92).

8. Claim 9 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

9. Claim 10 recites limitations that are substantially equivalent to those of Claim 2 and is rejected under similar reasoning.

10. Claim 11 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

11. In reference to Claim 12, Lindsay discloses the limitations as applied to Claim 10 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808) coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83).

12. In reference to Claim 13, Lindsay discloses the limitations as applied to Claim 12 above. Lindsay further discloses a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data (See Figure 8 Number 818 and Paragraph 83).

13. In reference to Claim 14, Lindsay discloses the limitations as applied to Claim 13 above. Lindsay further discloses that the plurality of buffers are connected between the

microcontroller and the Ethernet controller (See Figure 8 Number 818 and Paragraph 83).

14. In reference to Claim 15, Lindsay discloses the limitations as applied to Claim 12 above. Lindsay further discloses that the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller (See Paragraphs 83 and 84).

15. In reference to Claim 16, Lindsay discloses the limitations as applied to Claim 12 above. Lindsay further discloses a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller. (See Paragraph 80).

16. Claim 17 recites limitations that are substantially equivalent to those of Claim 4 and is rejected under similar reasoning.

17. Claim 18 recites limitations that are substantially equivalent to those of Claim 5 and is rejected under similar reasoning.

18. In reference to Claim 19, Lindsay discloses the limitations as applied to Claim 17 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808)

coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83).

19. In reference to Claim 20, Lindsay discloses the limitations as applied to Claim 19 above. Lindsay further discloses a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data (See Figure 8 Number 818 and Paragraph 83).

20. In reference to Claim 21, Lindsay discloses the limitations as applied to Claim 20 above. Lindsay further discloses that the plurality of buffers are connected between the microcontroller and the Ethernet controller (See Figure 8 Number 818 and Paragraph 83).

21. In reference to Claim 22, Lindsay discloses the limitations as applied to Claim 19 above. Lindsay further discloses that the Ethernet controller is configured to route ASF messages to an external ASF master (See Paragraphs 83 and 84).

22. In reference to Claim 30, Lindsay discloses the limitations as applied to Claim 9 above. Lindsay further discloses that the integrated circuit further comprises an ASF status register (See Figure 8 Number 824).

23. In reference to Claim 41, Lindsay discloses an external bus (See Figure 8 Number 802); an integrated circuit, comprising: an internal bus (See Figure 8 Number 811); a microcontroller (See Figure 8 Number 825) configurable as either an Alert Standard Format master or an Alert Standard Format slave (See Paragraphs 12-15 and 86), wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave (See Paragraph 90), wherein the microcontroller is further configured as an Advanced Configuration and Power Interface controller (See Paragraphs 74, 75, 83, and 96); and a bus interface logic connected to the external bus (See Figure 8 Number 806); and a processor coupled to the external bus.

24. In reference to Claim 42, Lindsay discloses the limitations as applied to Claim 41 above. Lindsay further discloses that the microcontroller is configured as the ASF master for the computer system (See Paragraph 90).

25. In reference to Claim 43, Lindsay discloses the limitations as applied to Claim 42 above. Lindsay further discloses an SMBus, one or more ASF devices coupled to the SMBus; and wherein the microcontroller is further configured to receive ASF status data from the one or more ASF devices over the SMBus (See Paragraph 91).

26. In reference to Claim 44, Lindsay discloses the limitations as applied to Claim 42 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808)

coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83); and wherein the processor is configured to communicate over a network with the Ethernet controller (See Paragraphs 83).

27. In reference to Claim 45, Lindsay discloses the limitations as applied to Claim 44 above. Lindsay further discloses that the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller (See Paragraphs 83 and 84).

28. In reference to Claim 46, Lindsay discloses the limitations as applied to Claim 44 above. Lindsay further discloses a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller. (See Paragraph 80).

29. In reference to Claim 47, Lindsay discloses the limitations as applied to Claim 41 above. Lindsay further discloses that the microcontroller is configured as the ASF slave (See Paragraph 90).

30. In reference to Claim 48, Lindsay discloses the limitations as applied to Claim 47 above. Lindsay further discloses that the microcontroller is configured to receive status

data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master (See Paragraph 92).

31. In reference to Claim 49, Lindsay discloses the limitations as applied to Claim 48 above. Lindsay further discloses a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as the Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card (See Figures 10 and 11).

32. In reference to Claim 50, Lindsay discloses the limitations as applied to Claim 47 above. Lindsay further discloses an Ethernet controller (See Figure 8 Number 808) coupled to the internal bus (See Figure 8 Number 811), wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus (See Paragraph 83).

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claims 6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to Claims 1 and 9 above, and further in view of what was well known in the art as exemplified by any one of US Patent Number 6,516,398 to Hwang ("Hwang"), US Patent Number 6,182,235 Ma et al. ("Ma"), and US Patent Number 5,742,833 to Dea et al. ("Dea").

35. In reference to Claim 6, Lindsay teaches the limitations as applied to Claim 1 above. Lindsay does not teach that the microcontroller is further configured as an embedded 8051 microcontroller. The Examiner takes Official Notice that embedded 8051 microcontrollers are well known in the art for controlling a variety of devices, including appliances and computer devices, evidence of which may be found in: Hwang (See Column 1 Lines 27-44); Ma (See Column 1 Lines 11-31); and Dea (See Column 4 Lines 1-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the use of an embedded 8051 microcontroller in the system of Lindsay, resulting in the invention of Claim 6, so as to take advantage of its widely recognized small size, low power consumption and versatility.

36. Claim 23 recites limitations that are substantially equivalent to those of Claim 6 and is rejected under similar reasoning.

37. Claims 7, 8, 24, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to Claims 1 above, and further in view of Applicant Admitted Prior Art ("AAPA").

38. In reference to Claims 7 and 8, Lindsay teaches the limitations as applied to Claim 1 above. Lindsay does not teach that the microcontroller is comprised in a bridge, as in Claim 7, and that the bridge is a south bridge, as in Claim 8. AAPA teaches an integrated circuit configured as a south bridge (See Figure 1A Number 112).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the microcontroller of Lindsay in the south bridge of AAPA, resulting in the inventions of Claims 7 and 8, because a south bridge provides an interface between various devices and subsystems and includes logic to interface with devices through the SMBus (See Page 3 Line 22 – Page 4 Line 4 of AAPA).

39. In reference to Claims 24 and 25, Lindsay teaches the limitations as applied to Claim 9 above. Lindsay does not teach that the integrated circuit is configured as a bridge, wherein the bridge further includes: a first bus interface logic for coupling to a first external bus; and a second bus interface logic for coupling to a second external bus, as in Claim 24, and that the bridge is configured as a south bridge, as in Claim 25. AAPA teaches an integrated circuit configured as a south bridge having first and second bus interface logic (See Figure 1A Number 112).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the microcontroller of Lindsay in the south bridge of AAPA, resulting in the inventions of Claims 7 and 8, because a south bridge provides an interface between various devices and subsystems and includes logic to interface with devices through the SMBus (See Page 3 Line 22 – Page 4 Line 4 of AAPA).

40. In reference to Claim 26, Lindsay and AAPA teach the limitations as applied to Claim 25 above. Lindsay further teaches a plurality of registers and a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bridge (See Figure 8 Number 824).

41. Claims 27, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to Claim 9 above, and further in view of US Patent Number 6,199,134 to Deschepper et al ("Deschepper").

42. In reference to Claims 27, 28, and 29, Lindsay teaches the limitations as applied to Claim 9 above. Lindsay does not teach a first embedded ACPI controller interface, as in Claim 27, a second embedded ACPI controller interface, as in Claim 28, and a third embedded ACPI controller interface, as in Claim 29. Deschepper teaches the use of embedded ACPI controller interfaces (See Abstract and Column 3 Line 55 – Column 4 Line 13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the microcontroller of Lindsay with the embedded ACPI controller interfaces of Deschepper, resulting in the inventions of Claims 27, 28, and 29, in order to allow components to be placed in a sleep mode to conserve power while still accurate data to be obtained from the component (See Column 3 Lines 18-30 and Column 4 Lines 49-65 of Deschepper).

43. Claims 55 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay, AAPA, and Deschepper.

44. In reference to Claim 55, Lindsay teaches receiving an Alert Standard Format message at a microcontroller (See Paragraphs 83 and 84). Lindsay further teaches that the device is an ACPI device (See Paragraphs 74, 75, 83, and 96). Lindsay does not teach receiving an ACPI event notification at the microcontroller; causing a system management interrupt to be generated using the microcontroller; and that the microcontroller is comprised in a south bridge. AAPA teaches an integrated circuit configured as a south bridge (See Figure 1A Number 112). Deschepper teaches a south bridge which receives an ACPI event notification and generates a system management interrupt (See Abstract and Column 3 Line 55 – Column 4 Line 13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the microcontroller of Lindsay in the south bridge of AAPA using the ACPI events and SMI signals of Deschepper, resulting in the inventions of

Claim 55, because a south bridge provides an interface between various devices and subsystems and includes logic to interface with devices through the SMBus (See Page 3 Line 22 – Page 4 Line 4 of AAPA) and to allow components to be placed in a sleep mode to conserve power while still accurate data to be obtained from the component (See Column 3 Lines 18-30 and Column 4 Lines 49-65 of Deschepper).

45. Claim 75 recites limitations that are substantially equivalent to those of Claim 55 and is rejected under similar reasoning.

Response to Arguments

46. Applicant's arguments filed 13 July 2006 have been fully considered but they are not persuasive.

47. Applicant has argued that Lindsay does not teach or suggest that the alerting network controller (Number 825) implements ACPI or operates according to ACPI. In response, the Examiner notes that Lindsay discloses that Figure 8 and Figure 7 are the same, except for the integration of components into controller 825 (See Paragraph 83). Lindsay further discloses that controller 700 (and likewise controller 800) effects management functionality through the use of the ACPI protocol (See Paragraphs 74-75). Thus, the components of controllers 700 and 800 operate according to the ACPI protocol. Lindsay further discloses that configuration application, which uses the ACPI

protocol for configuration, is used to configure ASF operation on the host system (See Paragraphs 92-94), and thus components of the system, such as controller 825, operate according to the ACPI protocol.

Conclusion

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thomas J. Cleary
Patent Examiner
Art Unit 2111